DS92LV16
Bus LVDS SERDES Demo Kit
User Manual

P/N BLVDS16EVK

Rev 2.31

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Network Interface Products

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Introduction

National Semiconductor's BLVDS16EVK evaluation board demonstrates the DS92LV16 BLVDS Serializer and Deserializer (SERDES) interface device.

This evaluation board verifies the:

- Serializer block that serializes the 16-bit parallel bus into a serial stream with embedded clock,
- Deserializer block that deserializes the serial data stream into a 16-bit parallel bus with associated clock,
- The BLVDS driver's line driving capability across a short Z-pack cable.

The serializer accepts up to sixteen 3V LVTTL/LVCMOS data signals from an incoming data source along with the clock (TCLK) and then converts the parallel signals into a single serialized BLVDS data stream. The deserializer recovers the BLVDS serialized data stream and converts it back into parallel 3VLVTTL/LVCMOS data and clock output signals. Note that the DS92LV16 serializer block and the deserializer block can operate independently of each other. The device also includes several test modes. By enabling the LINE LOOPBACK (LINE_LE) function, the signal integrity of the link may be checked.

Powering up the evaluation board is very simple. The user simply needs to provide the proper LVTTL/LVCMOS data inputs and clock to the serializer block, and the proper clock signal to the REFCLK input. The deserializer block features a random lock function, thus the serialized stream simply needs to be connected to the deserializer inputs and the recovered data and clock will be available at the output pins for monitoring / checking the random data. The deserializer may also be locked using the SYNC pin/function on the serializer.

National Semiconductor's DS92LV16 is intended to be used in mainly point-to-point applications. It should be terminated with 100Ω loads, or 50Ω loads with reduced margins.

Demo Kit Contents

- One demonstration board (BLVDS16PCB)
- One 1-meter AMP 2mm Hard Metric Z-pack cable
- BLVDS16EVK User Manual (this document)
- DS92LV16 Datasheet

EVK Features

- National Semiconductor's BLVDS DS92LV16 Serializer / Deserializer.
- Optional On-board 50MHz oscillator clock source.
- On-board LED for LOCK* indicator
- Configuration header pins for:
  - Power down controls
  - SYNC Pattern selection
  - Line and Local loopback enables for test modes
  - Output disable controls

Overview

The BLVDS16EVK SERDES demo board has independent 16-bit parallel input and output ports. J1 and J2 comprise the input pins and include 50Ω terminations to ground. J3 and J4 comprise the output pins. J5 provides access to all the control input signal pins and LOCK*pin. **Note that the odd number pins are connected to ground for J1 – J5.** A LED (D1) is provided on board for the user to monitor the status of the LOCK* indicator. A 50MHz oscillator (U2) is provided on board as an alternative REFCLK source. There are two pairs of differential signal lines connected to the 2mm Hard-Metric Header (P1B). The User can also utilize the Loopback test functions of the DS92LV16 to verify device operation. The signal function vs. connector / pin number are listed in table 1.

Table 1 (Signal Function vs Connector/Pin Number)

Signal Function	Connector	Pin number	Type
DIN0	J1	2	Data Input
DIN1	J1	4	Data Input
DIN2	J1	6	Data Input
DIN3	J1	8	Data Input
DIN4	J1	10	Data Input
DIN5	J1	12	Data Input
DIN6	J1	14	Data Input
DIN7	J1	16	Data Input
DIN8	J1	18	Data Input
DIN9	J1	20	Data Input
DIN10	J2	2	Data Input
DIN11	J2	4	Data Input
DIN12	J2	6	Data Input
DIN13	J2	8	Data Input
DIN14	J2	10	Data Input
DIN15	J2	12	Data Input
TCLK	J2	14	Serializer Clock Input
ROUT0	J3	2	Data Output
ROUT1	J3	4	Data Output
ROUT2	J3	6	Data Output
ROUT3	J3	8	Data Output
ROUT4	J3	10	Data Output
ROUT5	J3	12	Data Output
ROUT6	J3	14	Data Output
ROUT7	J3	16	Data Output
ROUT8	J3	18	Data Output
ROUT9	J3	20	Data Output

ROUT10	J4	2	Data Output
ROUT11	J4	4	Data Output
ROUT12	J4	6	Data Output
ROUT13	J4	8	Data Output
ROUT14	J4	10	Data Output
ROUT15	J4	12	Data Output
RCLK	J4	14	Deserializer Clock Output
TPWDN*	J5 / Header pin J6	2	Control Input
RPWDN*	J5 / Header pin J7	4	Control Input
DEN	J5 / Header pin J8	6	Control Input
REN	J5 / Header pin J9	8	Control Input
LOCAL_LE	J5 / Header pin J10	10	Control Input
LINE_LE	J5 / Header pin J11	12	Control Input
CONFIG1	J5 / Header pin J12	14	Control Input
CONFIG2	J5 / Header pin J13	16	Control Input
SYNC	J5 / Header pin J14	18	Control Input
LOCK*	J5 / LED – D1 and Header pin J20	20	Control Output
DO-	P1B	A1	Serializer's Differential Output (-)
DO+	P1B	B1	Serializer's Differential Output (+)
RIN-	P1B	D2	Deserializer's Differential Input (-)
RIN+	P1B	E2	Deserializer's Differential Input (+)
REFCLK	SMA - J17 / Header pin J15 and J16	N/A	Deserializer Frequency Reference Clock Input

The following sections explain each functional block of the DS92LV16 and the EVK.

Serializer Block

The Serializer block accepts up to sixteen LVTTL/LVCMOS (3V) data signals from an incoming data source along with the clock (TCLK) signal. These signals are serialized into the BLVDS data stream. The serial data stream includes a start bit and stop bit appended by the Serializer, which frames the sixteen data bits. The Serializer transmits the data and clock bits at 18 times (16 + 2 clock bits) the TCLK frequency. At 80MHz, the line rate is 1.44 Gbps, and the payload data rate is 1.28 Gbps.

The 18-bit parallel inputs are available at the 20-pin headers (J1, J2) on the board. **Note all odd pins on J1 and J2 are connected to GND.** The serialized differential data-out is available through header (P1B); see Differential Signals Connection and Termination for detail.

DIN0 to DIN9 – Pin (2, 4, 6, 8, 10, 12, 14, 16, 18, 20) of J1

Serializer data inputs. The serializer data signals must be driven from a source with 3V logic levels. Input pins are not 5V tolerant.

Note some test equipment may require a 50Ω termination on these pins. These pins include termination resistors (R1 – R10) on the board for this purpose.

DIN10 to DIN15 – Pin (2, 4, 6, 8, 10, 12) of J2

Serializer data inputs. The serializer data signals must be driven from a source with 3V logic levels. Input pins are not 5V tolerant.

Note some test equipment may require a 50Ω termination on these pins. These pins include termination resistors (R11 – R16) on the board for this purpose.

TCLK – Pin 14 of J2

The TCLK pin drives the serializer PLL and is used to strobe data at the DIN inputs. The clock signal should be within the operating frequency of the device (125MHz – 80MHz) and it is important that the clock signal source be driven with a 3V logic signal. The inputs are not 5V tolerant.

Note some test equipment may require a 50Ω termination on this pin. This pin includes a termination resistor pad (R17) on the board.

TPWDN* – Pin 2 of J5 and Header pin J6

The serializer power down function can be controlled two ways. A header pin (J6) is available for pulling the signal High, or it may be driven through pin 2 of J5. The following states are possible:

- J6 Tied to HIGH will cause the Serializer block to enable.
- J6 Open will connect the device's TPWDN* pin to Pin 2 of J5.
- J6 Tied to LOW will cause the Serializer block to power down.

When TPWDN* is driven LOW, the PLL of the serializer will lose lock, the output of the serializer will enter TRI-STATE, and the supply current will drop into the μA range. When TPWDN* is driven HIGH, the Serializer is enabled and will operate as indicated by the other control and input pins.

DEN – Pin 6 of J5 and Header pin J8

The DEN pin controls the serializer's outputs. The serializer outputs will enter TRI-STATE when the DEN pin is LOW. When DEN is HIGH, the outputs are active. A header pin (J8) is available for pulling the signal High, or it may be driven through pin 6 of J5. The following states are possible:

- J8 Tied to HIGH) will enable the serializer outputs.
- J8 Open will connect the device's DEN pin to Pin 6 of J5.
- J8 Tied to LOW will disable the serializer outputs and cause the outputs to enter TRI-STATE.

SYNC – Pin 18 of J5 and Header pin J14

The SYNC pin enables the SYNC function of the serializer. By enabling the SYNC function, the serializer transmits the special synchronization pattern (sync-pattern). The sync-pattern is a fixed pattern consisting of 9-bits high and 9-bits low as shown in the datasheet. Logic HIGH on this pin will force the sync-patterns to be sent per datasheet details and a logic LOW places the serializer in normal operation mode. A header pin (J14) is available for pulling the signal High, or it may be driven through pin 18 of J5. The following states are possible:

- J14 Closed (HIGH) will cause the serializer to output sync-patterns.
- J14 Open will connect the device's SYNC pin to Pin 18 of J5.
- J14 Open and a no connect on Pin 18 of J5 will place the serializer in normal operation mode.

Note: the SYNC pin is internally pulled-low; as a result, when the SYNC pin is a left floating, the device is in normal operation mode.

Deserializer Block

The Deserializer block recovers the BLVDS data stream back into LVTTL/LVCMOS parallel data and clock. During synchronization, the Deserializer's PLL uses the Reference Clock (REFCLK) as a frequency reference to lock to the incoming BLVDS data stream. After the Deserializer's PLL locks to the embedded clock, the LOCK* pin goes low and valid data and clock will appear on the deserializer outputs.

The 16-bit parallel outputs are available at the 20-pin headers (J3, J4) on the board. **Note: all odd pins on J3, J4 are connected to GND.** The serialized differential data-in is applied through header (P1B); see the section titled "Differential Signals Connection and Termination" for details.

ROUT0 to ROUT9 - Pin (2, 4, 6, 8, 10, 12, 14, 16, 18, 20) of J3

Deserializer parallel data outputs. These pins are LVCMOS level.

Note: 0805 pads in series (R18 – R27, default are shorted out) are provided if the user needs to install 450Ω series resistors. This is required if directly connecting to a 50Ω input on a scope. The pad is unpopulated from the factory and in order to use this option, the user must cut the signal line between the pads before installing the 450Ω series resistors.

ROUT10 to ROUT15 - Pin (2, 4, 6, 8, 10, 12) of J4

Deserializer parallel data outputs. These pins are LVCMOS level.

Note: 0805 pads in series (R28 – R33, default are shorted out) are provided if the user needs to install 450Ω series resistors. This is required if directly connecting to a 50Ω input on a scope. The pad is unpopulated from the factory and in order to use this option, the user must cut the signal line between the pads before installing the 450Ω series resistors.

RCLK – Pin 14 of J4

RCLK is the Recovered Clock of the deserializer block. This LVCMOS/LVTTL output signal contains information of the parallel data rate clock recovered from the serial data stream. The RCLK signal is used to strobe the ROUT data.

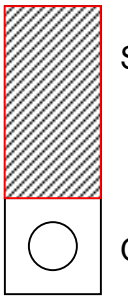
Note: an 0805 pad in series (R34, default is shorted out) is provided if the user needs to install a 450Ω series resistor. This is required if directly connecting to a 50Ω input on a scope. The pad is unpopulated from the factory and in order to use this option, the user must cut the signal line between the pads before installing the 450Ω series resistor.

REFCLK – Header pin J15 / SMA – J17 / Header pin J16

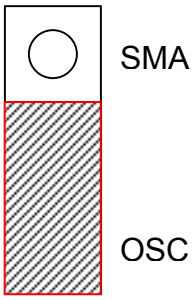
The REFCLK input is used as a frequency reference to the deserializer's PLL. Its frequency must be within +/-5% of the TCLK signal frequency and it has no phase relationship with the deserializer output.

User may either select the on-board 50 MHz oscillator and operate the device at 50 MHz or apply an external clock for the REFCLK. Selection of clock source is accomplished using REFCLK CONTROL (header pin J15). The following states are possible:

- Connecting J15 to SMA will tie the device REFCLK pin to the SMA connector (J17). When using external clock to drive REFCLK signal, the user supplies the clock signal to the SMA connector (J17) on the board. The signal source must be:
  - Driven with a signal of 3.3V
  - Capable of driving a 50Ω resistive load. When selected for external clock source, the board presents a 50Ω (R49) termination to GND for the user's signal generator.
- Connecting J15 to OSC will tie device REFCLK pin to the on-board 50 MHz oscillator (U2). The user must leave header pin J16 OPEN to enable the oscillator. When J16 is CLOSED, the oscillator will be disabled. Note that this is a 3.3V device. **When the on-board 50 MHz oscillator is used as the supply for the REFCLK signal, the signal source driving the TCLK signal must also be at 50 MHz. See clock tolerance requirements (5%) in the datasheet.**



(REFCLK driven by signal applied through SMA –J17)



(REFCLK driven by oscillator U2)

RPWDN* – Pin 4 of J5 and Header pin J7

The deserializer power down function can be controlled two ways. A header pin (J7) is available for pulling the signal HIGH, or it may be driven through pin 4 of J5. The following states are possible:

- J7 Tied to HIGH will enable the Deserializer block.
- J7 Open will connect the device's RPWDN* pin to Pin 4 of J5.
- J7 Tied to LOW will cause the Deserializer block to power down.

When RPWDN* is driven LOW, the PLL of the deserializer will lose lock, the output of the deserializer will go into TRI-STATE, and the supply current will drop into the μA range. When RPWDN* is driven HIGH, the deserializer is enabled and will operate as indicated by the other control and input pins.

REN – Pin 8 of J5 and Header pin J9

The REN pin controls the deserializer outputs. The deserializer outputs will enter TRI-STATE when the REN pin is LOW. When REN is HIGH, the outputs are active. A header pin (J9) is available for pulling the signal High, or it may be driven through pin 8 of J5. The following states are possible:

- J9 Tied to HIGH will enable the deserializer outputs.
- J9 Open will connect the device's REN pin to Pin 8 of J5.
- J9 Tied to LOW will disable the deserializer outputs.

LOCK* – LED –D1 / Pin 20 of J5

The LOCK* pin indicates the status of the deserializer block PLL. The user can monitor this pin to see whether the deserializer has locked to the BLVDS data stream.

- LOCK* = HIGH (LED = ON): deserializer's PLL = unlocked; RCLK and ROUT data are invalid.
- LOCK* = LOW (LED = OFF): deserializer's PLL = locked; RCLK ROUT data is valid.

The status of the LOCK* pin can be monitored by either probing pin 20 of J5 or by monitoring the state of LED-D1.

Note: the LOCK* LED CONTROL (header pin J20) must be CLOSED in order to enable D1.

Power Supply Connection

Power and Ground must be applied through power terminals J18 and J19. They are the main power supply connection for the EVK. Ground should be applied to J18 and 3.3V +/-4.5% should be applied to J19.

Option – Loopback Test

The DS92LV16 includes two test modes for testing the functionality of the device and the transmission line continuity. They are LOCAL Loopback mode and LINE Loopback mode. Please see the datasheet for details.

LOCAL_LE – Pin 10 of J5 and Header pin J10

The LOCAL_LE pin controls the LOCAL Loopback test that enables the user to check the integrity of the transceiver from the local parallel-bus. By enabling the LOCAL Loopback mode, the parallel data inputs (DIN [0:15]) loop back to the parallel data outputs (ROUT [0:15]) post serialization. The connection route includes all the functional blocks of the Transceiver. The serial data outputs (DO+/-) are automatically disabled during the LOCAL Loopback mode. The following states are possible:

- J10 Tied to HIGH will cause the device to go into LOCAL Loopback mode.
- J10 Open will connect the device's LOCAL_LE pin to Pin 10 of J5.
- J10 Tied to LOW will cause the device to operate as indicated by the other control and input pins.

LINE_LE – Pin 12 of J5 and Header pin J11

The LINE_LE pin controls the LINE Loopback test mode that enables the user to check transmission line continuity. By enabling the LINE Loopback mode, the serial data inputs (RIN+/-) connect to the serial data outputs (DO+/-) in addition to the parallel data outputs (ROUT [0:15]). The following states are possible:

- J11 Tied to HIGH will cause the device to go into LINE Loopback mode.
- J11 Open will connect the device's LINE_LE pin to Pin 12 of J5.
- J11 Tied to LOW will cause the device to operate as indicated by the other control and input pins.

CONFIG1 – Pin 14 of J5 and Header pin J12

This pin corresponds to pin #3 (CONFIG 1) of the device. Users are required to pull this pin (J12) to HIGH. LOW reserved for future use.

CONFIG2 – Pin 16 of J5 and Header pin J13

This switch corresponds to pin #18 (CONFIG 2) of the device. Users are required to pull this pin (J13) to HIGH. LOW reserved for future use.

Setting up BLVDS16EVK

There are many ways to set up this EVK for bench testing and performance measurements. The following are just a few of the many ways to set up the kit.

Quick check for EVK

The user can perform the following to ensure the functionality of the EVK:

1) Apply a 3.3V +/-4.5% to Power Terminal J19 and apply ground to Power Terminal J18.

2) Connect one end of the AMP 2mm Z-pack cable to row 1 of the 2mm Hard Metric Header (P1B) on the board and the other end to row 2 of P1B on the same board.

3) Tied the following header pins on the board to HIGH:
   TPWDN* (J6)
   RPWDN* (J7)
   DEN (J8)
   REN (J9)
   CONFIG1 (J10)
   CONFIG2 (J11)
   SYNC (J12)
   LOCK* LED CONTROL (J14)

   Note: The demo kit comes fully loaded with all configuration jumpers connected. Unused modes should have their jumpers removed.

4) Apply a 50MHz, LVTTL/LVCMOS (3V) clock signal from a clock source (signal generator, BERT tester, etc) to the TCLK (pin 14 of J2).

5) Tie REFCLK CONTROL (J15) to OSC. Make sure jumper J63 is open.

6) Monitor the state of the LOCK* INDICATOR LED (D1). If the LED is NOT ON, the EVK is functioning properly and the serializer and deserializer are synchronized.

External loopback data transfer setup

The user can also use the following setup to perform a Bit-Error-Rate Test and a quick check of the LVDS signal.

1) Apply a 3.3V +/-4.5% to Power Terminal J19 and apply ground to Power Terminal J18.

2) Connect one end of the AMP 2mm Z-pack cable to row 1 of the 2mm Hard Metric Header (P1B) on the board and the other end to row 2 of P1B on the same board.

3) Close the following header pins on the board:
   TPWDN* (J6)
   RPWDN* (J7)
   DEN (J8)
   REN (J9)
   CONFIG1 (J12)
   CONFIG2 (J13)
   LOCK* LED CONTROL (J14)

4) Apply a LVTTL/LVCMOS (3V) clock signal from a clock source (signal generator, BERT tester, etc) to TCLK (pin 14 of J2)

   Note: the TCLK signal should be between 25 and 80 MHz.

5) Apply a LVTTL/LVCMOS (3V) data signal from a data source (signal generator, BERT tester, etc) to the two DIN signal connectors on the board (J1, J2). See Table 1 for the pin mapping of J1 and J2.

6) Tie REFCLK CONTROL (J15) to SMA

7) Apply a LVTTL/LVCMOS (3V) clock signal from a clock source to the REFCLK pin via the SMA connector (J17) on the board.

   Note: the frequency of the signal applied to REFCLK must be within +/-5% of the TCLK signal frequency.

8) Data applied to the inputs are now serialized, transmitted, deserialized and re-driven to the deserializer outputs (ROUT [0:15]). The user can also monitor the integrity of the LVDS signal by probing the LVDS signal probe-points on the board.

Typical Connection / Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX LVTTL/LVCMOS inputs:

1) TEK HFS9009 – This pattern generator along with 9DG2 Cards may be used to generate input signals and the clock signal.
2) TEK DG2020 – This generator may also be used to generate data and clock signals.
3) TEK MB100 BERT – This bit error rate tester may be used for both signal source and deserializer.
4) Any other signal / pattern generator that generates the correct input levels as specified in the DS92LV16 datasheet.

The following is a list of typical test equipment that may be used to monitor the output signals from the Rx LVTTL/LVCMOS outputs:

1) TEK MB100 BERT – Deserializer.
2) Any oscilloscope with 50Ω inputs (used in conjunction with the optional 450Ω series resistor pads on the board) or with high impedance probes.

LVTTL/LVCMOS signals to the EVK can be connected to the pattern generator / oscilloscope with any pin header cable. The following is the cable that was used in testing: Tektronix SMB-pin header cable (20in), P/N:012150300

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the **TEK P6247**, **P6248**, or **P6330** differential probes.

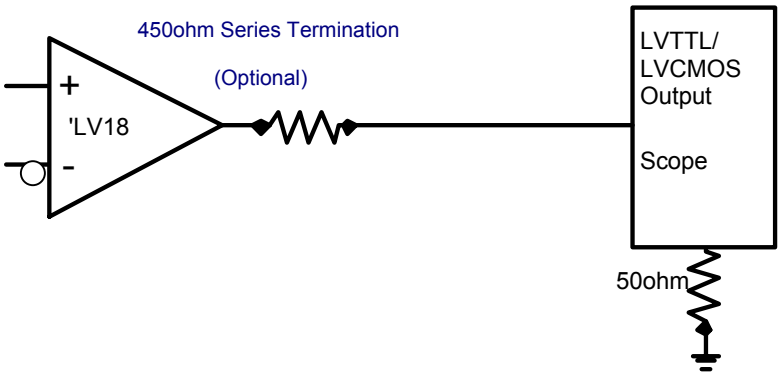
LVCMOS/LVTTL Termination (Options)

Pads are provided for output signal attenuation for compatibility with 50Ω scope heads. For parallel outputs, series 450Ω resistors can be added for compatibility with 50Ω scope inputs **(**see Table 2 and Figure 1). These resistor locations are labeled R20- R38.

Note: the output series resistor pads are shipped with a shorting trace. To use the series resistor option, the trace must be cut between the mounting pads prior to installing a resistor.

Table 2 and Figure 1

LVCMOS/LVTTL OUTPUT	Series Termination Resistor
ROUT0	R18
ROUT1	R19
ROUT2	R20
ROUT3	R21
ROUT4	R22
ROUT5	R23
ROUT6	R24
ROUT7	R25
ROUT8	R26
ROUT9	R27
ROUT10	R38
ROUT11	R29
ROUT12	R30
ROUT13	R31
ROUT14	R32
ROUT15	R33
RCLK	R34

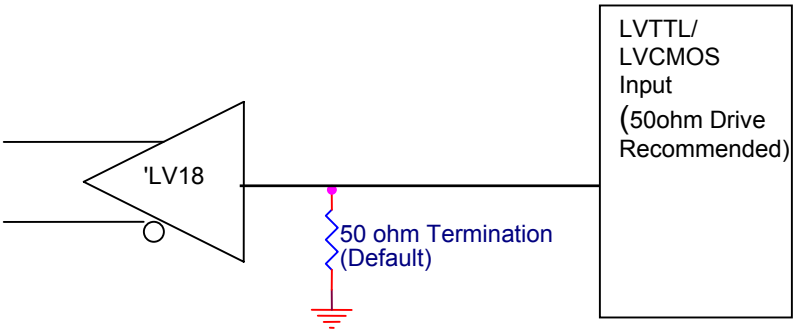


LVCMOS/LVTTL Termination (Default)

For parallel inputs, 50Ω termination resistors to GND are included on the board (see Table 3 and Figure 2). These resistor locations are labeled R1-R19.

Table 3 and Figure 2

LVCMOS/LVTTL INPUT	Termination Resistor
DIN0	R1
DIN1	R2
DIN2	R3
DIN3	R4
DIN4	R5
DIN5	R6
DIN6	R7
DIN7	R8
DIN8	R9
DIN9	R10
DIN10	R11
DIN11	R12
DIN12	R13
DIN13	R14
DIN14	R15
DIN15	R16
TCLK	R17

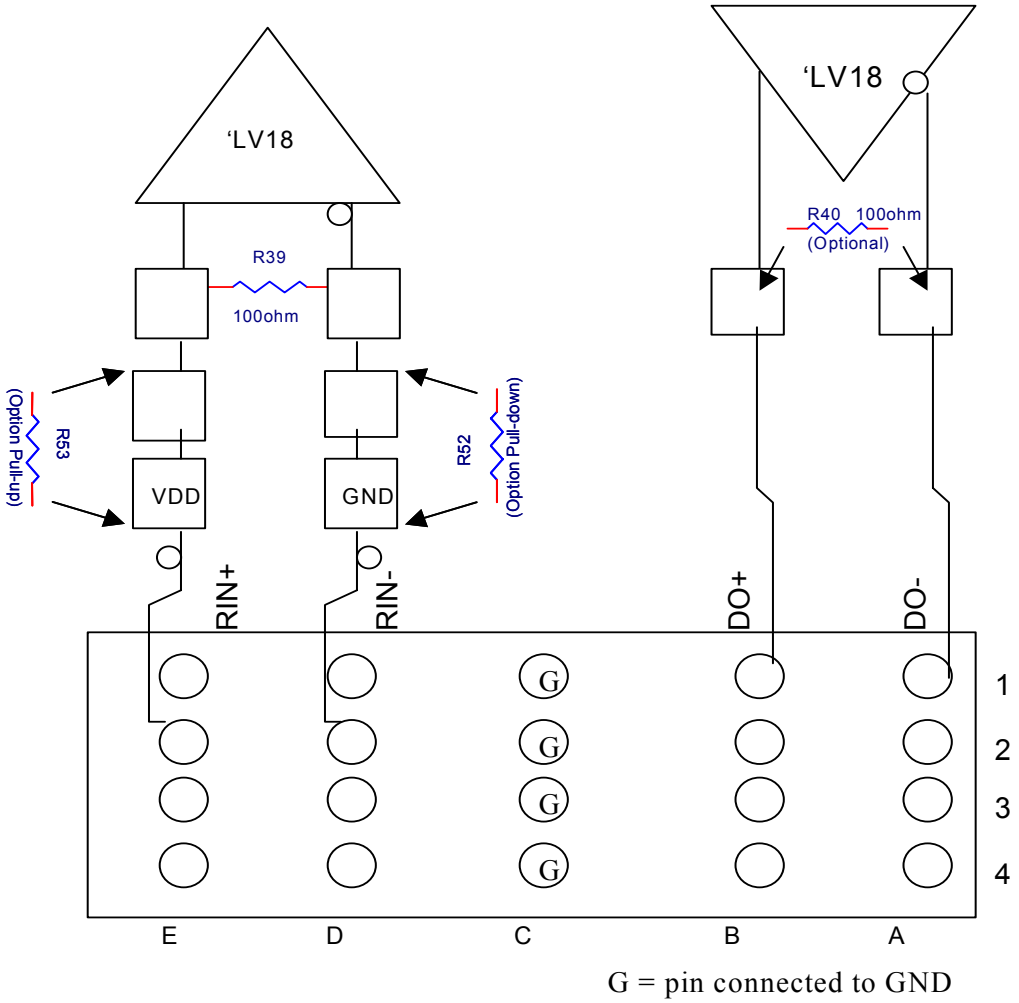


Differential Signals Connection and Termination

Differential signals connection can be found at the 2mm Hard-Metric Header (P1B). The user can access the serializer differential outputs on pins A1 (DO+) and B1 (DO-) of P1B. Connection to the deserializer's differential inputs can be found on pins D2 (RIN-) and E2 (RIN+) of P1B. Two probing points are available at the deserializer's differential inputs for the user to monitor the integrity of the differential input signal. Plese see Figure 3.

A 100-Ω termination resistor (R39) is provided at the deserializer inputs (RIN +/-) and an optional unpopulated resistor pad (R40) is provided at the serializer outputs (DO+/-), so the user can add a differential termination resistor on the serializer output if needed. In addition, a couple of unpopulated pads (R52 and R53) are provided at the deserializer inputs (RIN +/-) for optional failsafe biasing. Please see Figure 3 and the schematic for the location of these terminations.

Figure 3



G = pin connected to GND

Additional Information

For more information on BLVDS Serializers / Deserializers, please refer to National's LVDS website at:

www.national.com/appinfo/lvds

Interface Applications Hotline:

The Interface Hotline number is: +1 408 721-8500

Appendix

AMP's 2mm Hard-Metric Connector and Z-pack Cable

AMP cable/ connector specifications and drawings are available at:

www.amp.com

PART NUMBER: 352041-7

Demo Board PCB Schematic

Document available upon request. Please ask for:

BLVDS16PCB_rev2.2.pdf

Demo Board PCB Bill-of-Material

Document available upon request. Please ask for:

BLVDS16BOM_rev2.2.pdf